Influence of a SVC on AC Arc Furnaces Harmonics, Flicker and Unbalance. Measurement and analysis.

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Abstract-An AC arc furnace is an unbalanced, nonlinear and time varying load, which can cause many problems to power system quality. Different studies on arc furnaces harmonics analysis can be found in the bibliography on the topic; however, it is very difficult obtain an exact model that takes into account all the parameters that have influence on the process, therefore it is necessary to take measurements under different conditions. In this paper we'll present the harmonic distortion, flicker and unbalance results and conclusions on three different measurement campaigns in an iron and steel industry (SNL) with an AC arc furnace of 83 MW (170 TM) with a transformer of 120 MVA connected with a dedicated power line of 220 kV (55 km) to the Carregado Substation, where there are another other branches that connect industrial and domestic consumers.

Keywords: Flicker, harmonics, power quality, electric power measurements, arc furnaces.

I. INTRODUCTION

Harmonics, inter-harmonics, voltage flicker and unbalance are the power quality problems which are introduced in a power system as a result of the nonlinear and stochastic behaviour of the arc furnace operation. The nonlinear voltage-current characteristic of the arc can cause harmonic currents which, when circulating over the network, can produce harmonic voltages which can affect other users.

The furnace shell is isolated and it is represented by a star connection of the three arcs, so that if a three-phase arc furnace operation was balanced, the zero sequence components of the current wave would be null. Actually, unbalanced operation is the normal situation in the meltdown process and this produces zero sequence harmonics in the arc current. However, due to the influence between phases, these harmonic components do not reach the values that we would find in the current wave of a single-phase operation arc.

Different studies on arc furnaces harmonics analysis can be found in the bibliography on the topic, for example, in [1] an arc model is presented, to carry out harmonic analysis of an AC three-phase arc furnace with a single-phase circuit. This model is based on V-I characteristic of the arc and takes into account the effect of the arc's unbalance over the zero sequence harmonics.

Nevertheless, taking into account that the arc melting process is a stationary stochastic process, it is difficult to obtain an accurate model for an arc furnace load. The factors that affect the arc furnace operation are the melting materials, the electrode position, the electrode arm control scheme, and the system voltage and impedance. For all these reasons, it is very important to take measurements.

The solution to improve the energy quality (PQ-Power Quality) at the load point is of great important when the production process gets more complicated and requires a bigger reliability level, which includes objectives such as providing energy without interruptions, without harmonic distortion and with voltage kept in a very narrow margin. The devices that can fulfil these requirements are the Custom Power; a concept that we could include among the FACTS, but that is different because of their final use. In fact, the topologies used are identical those of FACTS devices with little modifications and adaptations to voltage levels, therefore they are mostly oriented to be used in distribution networks of low and medium tension, sometimes replacing active filters.

II. ELECTRICAL CIRCUIT

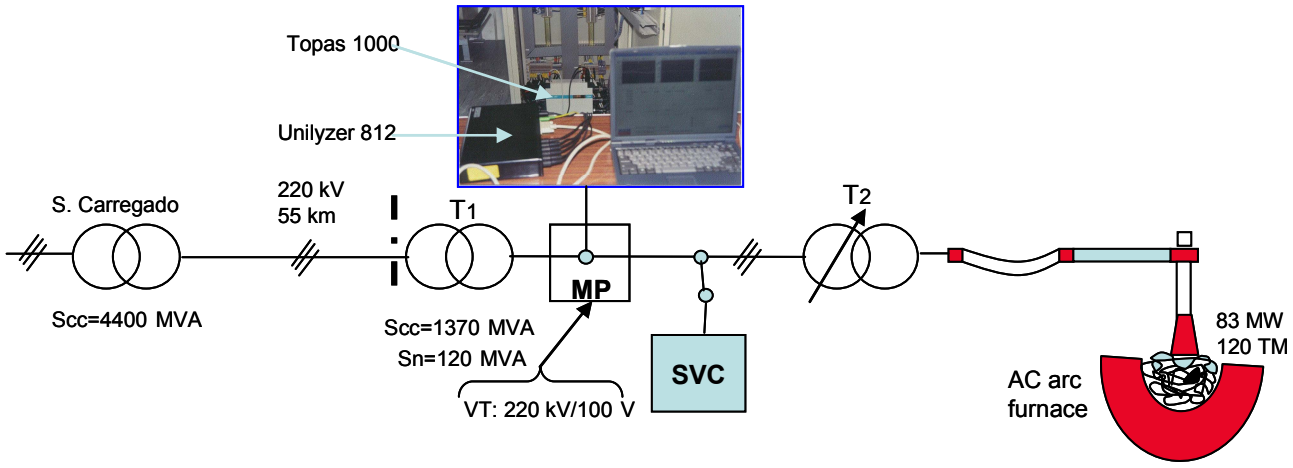


Figure 1. Electrical circuit chart of the AC arc furnace supply from Carregado Substation with the measurement equipment

III. SIMULATION

For the simulation we applied a PSIM package with a model represented in Fig. 2, which is justified along this point and some of the results, for input and output currents, are presented in Fig. 10.

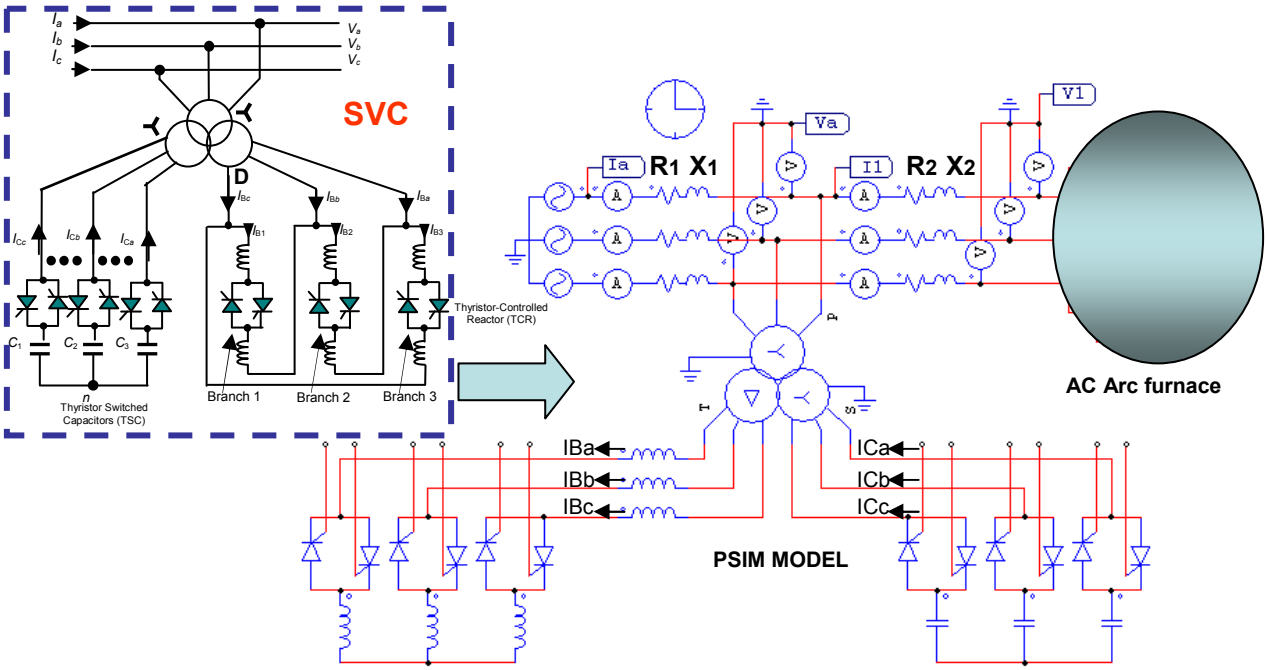


Figure 2. Representation of a three-phase static VAR compensator (SVC) comprising a thyristor-controlled reactor (TCR) and a thyristor-switched capacitor (TSC) with his PSIM model.

Concerning the three-phase thyristor-controlled reactor (TCR) it is not difficult to see from the expression for the fundamental frequency current, Equation (1), that a part of it can be interpreted as the equivalent susceptance, which is a function of the controlled parameter α [7]. Then Equation (1) may be expressed by equation (2):

$$I_B = \frac{V}{j\omega L\pi}\left[2(\pi-\alpha)+\sin 2\alpha\right] \quad (1)$$

$$I_B = -jB_e V \quad (2)$$

Where: $$B_e = \frac{2(\pi-\alpha)+sen2\alpha}{\pi\omega L} \quad (3)$$

Using the results in Equation (2) for the case of a three phase TCR, Figure (4), we have Equation (4)

$$\begin{bmatrix} I_{B1} \\ I_{B2} \\ I_{B3} \end{bmatrix} = \begin{bmatrix} -jB_{e1} & 0 & o \\ 0 & -jB_{e2} & 0 \\ 0 & 0 & -jB_{e3} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad (4)$$

and the connectivity matrices for phases a,b,c. Equations (5) and (6).

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \frac{(\pi/6)}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} I_{Ba} \\ I_{Bb} \\ I_{Bc} \end{bmatrix} = \frac{(-\pi/6)}{\sqrt{3}} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} I_{B1} \\ I_{B2} \\ I_{B3} \end{bmatrix} \quad (6)$$

Substituting Equation (5) into Equation (4), and the intermediate result into Equation (6), we obtain Equation (7), that represents the phase domain equivalent circuit for the six-pulse three phase TCR of Figure 2.

$$\begin{bmatrix} I_{Ba} \\ I_{Bb} \\ I_{Bc} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} -j(B_{e1}+B_{e3}) & jB_{e1} & jB_{e3} \\ jB_{e1} & -j(B_{e1}+B_{e2}) & jB_{e2} \\ jB_{e3} & jB_{e2} & -j(B_{e2}+B_{e3}) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (7)$$

If all the three branches in the TCR have an equal equivalent $B_{e1} = B_{e2} = B_{e3} = B_e$, which depends on the design of the circuit, then Equation (7) simplifies to Equation (8).

$$\begin{bmatrix} I_{Ba} \\ I_{Bb} \\ I_{Bc} \end{bmatrix} = j\frac{1}{3}B_e \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (8)$$

An alternative representation of Equation (8) becomes feasible, using the reference frame provided by the concept of symmetrical components. The transformation from phase coordinates to sequence coordinates involves applying the matrix of symmetrical components [a] and its inverse to Equation (8), leading to Equation (9).

$$\begin{bmatrix} I_{B0} \\ I_{B1} \\ I_{B2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -jB_e & 0 \\ 0 & 0 & -jB_e \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \quad (9)$$

In Equation (9) three sequence components are associated with three-phase circuits, namely zero (0), Positive (1), and negative (2), sequences.

If equal equivalent admittances may be assumed in the six-pulse TCR then the positive sequence representation becomes Equation (10).

$$I_{B1} = -jB_e V_1 \quad (10)$$

The nodal admittance of the capacitor bank, in phase coordinates, may be expressed with explicit representation of the Stara point, which is not grounded. However, it is more advantageous to perform a Kron reduction to obtain a reduced equivalent, where only the parameters of phases a,b, and c are represented explicitly.

In the most general case, with $B_{C1} \neq B_{C2} \neq B_{C3}$, and after performing Kron's reduction, the reduced equivalent model of the thyristor switched capacitor (TSC) is represented by the Equation (11).

$$\begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} = \begin{bmatrix} j\left(B_{C1} - \frac{B_{C1}^2}{\Delta B_C}\right) & -j\frac{B_{C2}B_{C1}}{\Delta B_C} & -j\frac{B_{C3}B_{C1}}{\Delta B_C} \\ -j\frac{B_{C1}B_{C2}}{\Delta B_C} & j\left(B_{C2} - \frac{B_{C2}^2}{\Delta B_C}\right) & -j\frac{B_{C3}B_{C2}}{\Delta B_C} \\ -j\frac{B_{C1}B_{C3}}{\Delta B_C} & -j\frac{B_{C2}B_{C3}}{\Delta B_C} & j\left(B_{C3} - \frac{B_{C3}^2}{\Delta B_C}\right) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (11)$$

Where:

$$\Delta B_C = B_{C1} + B_{C2} + B_{C3} \qquad \begin{aligned} B_{C1} &= \varpi C_1 \\ B_{C2} &= \varpi C_2 \\ B_{C3} &= \varpi C_3 \end{aligned} \quad (12)$$

If all the branches of TSC have equal equivalent susceptances: $(B_{C1} = B_{C2} = B_{C3} = B_C)$, then Equation (11) simplifies to Equation (13).

$$\begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} = j\frac{1}{3}B_C \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (13)$$

The most general expression for the six-pulse SVC would be the case when Equation (7) and Equation (11) are added together, providing a model where SVC design imbalances may be accounted for.

A more constrained, but still very useful, model, is the case when Equation (8) and Equation (13) are used as the constituent part of the SVC model, Equation (14).

$$\begin{bmatrix} I_{SVCa} \\ I_{SVCb} \\ I_{SVCc} \end{bmatrix} = \begin{bmatrix} I_{Ca} \\ I_{Cb} \\ Icc \end{bmatrix} + \begin{bmatrix} I_{Ba} \\ I_{Bb} \\ I_{Bc} \end{bmatrix} = \frac{1}{3}j(B_C - B_e) \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_C \end{bmatrix} \quad (14)$$

The SVC model given by Equation (14) is suitable for deriving a representation in the reference frame of symmetrical components, Equation (15).

$$\begin{bmatrix} I_{SVC0} \\ I_{SVC1} \\ I_{SVC2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & j(B_C - B_e) & 0 \\ 0 & 0 & j(B_C - B_e) \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \quad (15)$$

Similar to TCR, non zero sequence current can flow in the SVC circuit as the star point of the TSC is not grounded. The positive sequence ands negative sequence circuits contain equal impedances. However, for cases of balanced operation and balanced SVC designs only the positive sequence representation is of interest

$$I_{SVC1} = jB_{SVC} V_1 \quad (16)$$

Where:

$$B_{SVC} = B_C - B_e = \frac{1}{X_C X_L}\left\{X_L - \frac{X_C}{\pi}[2(\pi - \alpha)] + sen2\alpha\right\}$$

$$X_L = \varpi L \quad (17)$$

$$X_C = \frac{1}{\varpi C}$$

It should be remarked that the positive sequence model of the SVC, Equation (16), should also serve the purpose of representing a single-phase SVC

Model of the arc furnace

Figure 3 shows the electrical model for the arc furnace where the outer non-linear resistances (inter-electrode resistances) form a delta-circuit with the three nodes. The inner resistances (slag-to-matte resistances) form a wye-connection with Vm as a virtual ground (floating neutral point).

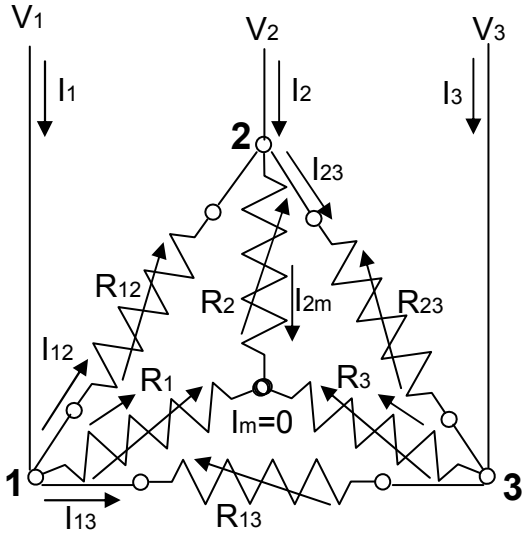


Figure 3. Electrical model of the arc furnace

Figure 3 shows four nodes, one for each of the electrodes and the fourth representing the virtual ground at the matte (Vm). Using these nodes, it is possible to determine the current in each electrode with respect to each voltage and the conductance coefficients, using its position as the input. Proper assumptions can facilitate derivations thus calculating the Equation (18) involving matrices [8].

$$[I_i] = [G_{ij}][x_i] + [B_i] \quad (18)$$

Here I_i is a 3x1 matrix with electrode currents, G_{ij} is a 3x3 conductance matrix, x_i is a 3x1 matrix that represent the immersion depth of each electrode in the slag and B_i is a 3x1 constant matrix.

The following set of equations can be obtained by applying Kirchoff's Current Law to each of the four nodes displayed in Figure 5.

$$I_1 = G_{12}(V_1 - V_2) + G_1(V_1 - V_m) + G_{13}(V_1 - V_3)$$
$$I_2 = -G_{12}(V_1 - V_2) + G_2(V_2 - V_m) + G_{23}(V_2 - V_3)$$
$$I_3 = G_3(V_3 - V_m) - G_{13}(V_1 - V_3) + G_{23}(V_2 - V_3)$$
$$G_1(V_1 - V_m) + G_2(V_2 - V_m) + G_3(V_3 - V_m) \quad (19)$$

Where:

$$V_m = \frac{G_1V_1 + G_2V_2 + G_3V_3}{G_1 + G_2 + G_3} \quad (20)$$

In reference [8] the calculation of the currents of the three phases I_1, I_2 and I_3 can be found.

The authors of [8] consider that the inter-electrode resistances are equivalent, but in our simulations by PSIM we consider that all the resistances modelling the AC arc furnace, Fig. 3, are different, non linear and all of the resistances depend on the voltage and electrodes position. The electrical circuit is represented by Fig. 4 or, in a simplified version, by Fig. 5, in which the resistances and reactances are the same as those that appear at Fig.2.

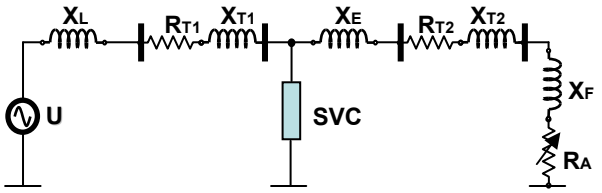


Figure 4. Electrical equivalent circuit of the total system where R_A represents the electrical model of the arc furnace

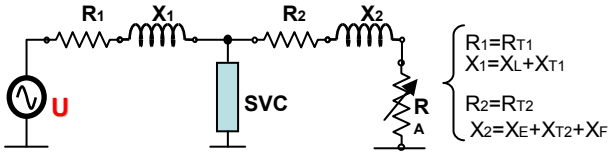


Figure 5. Electrical equivalent circuit of the total system, where R_A is represented by Figure 3 and the resistances and reactances are the same as those of Figure 2.

IV. MEASUREMENTS RESULTS

TABLE 1. Summary of the flicker Pst 95% at the measurement point in SN Longos and at the Carregado Substation. Measurement campaign from 9th to 13th February (without SVC) and from 16th to 20th February (with SVC).

Pst 95 FLICKER SNL MEASUREMENTS FROM 9th TO 13th (without SV) AND FROM 16th TO 20th (with SVC) OF FEBRUARY										
DAY	D 9	D 10	D 11	D 12	D 13	D16	D17	D18	D19	D20
PHASE 1	0,125	6,031	6,313	6,031	5,938	0,156	2,906	3,281	3,313	3,280
PHASE 2	0,156	5,750	6,313	6,375	5,781	0,156	2,844	3,281	3,313	3,219
PHASE 3	0,125	5,688	5,625	5,688	5,188	0,188	2,750	3,031	3,156	3,094
	Pst 95 FLICKER TRANSMITTED TO CARREGADO SUBSTATION									
PHASE 1	0,039	1,878	1,965	1,878	1,849	0,049	0,905	1,022	1,031	1,021
PHASE 2	0,049	1,775	1,965	1,985	1,800	0,049	0,885	1,022	1,031	1,002
PHASE 3	0,039	1,771	1,751	1,771	1,615	0,058	0,856	0,944	0,983	0,963

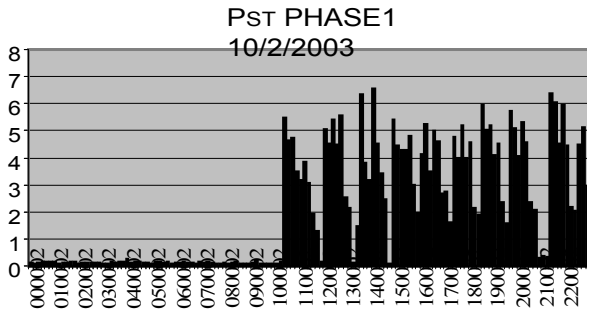


Figure 6. Chart of the short term flicker (Pst) of phase 1 without SVC; the arc furnace working at 30 MW.

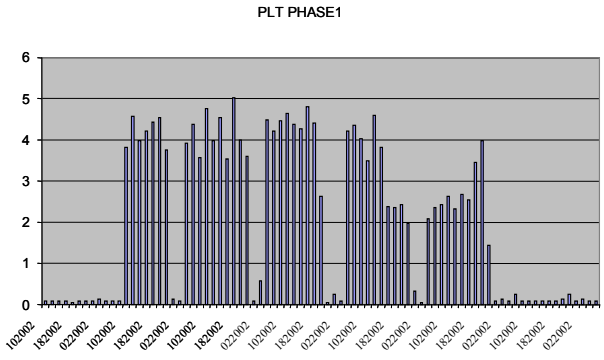


Figure 7. Chart of the long term flicker (Plt) of phase 1 without SVC; arc furnace working at 30 MW.

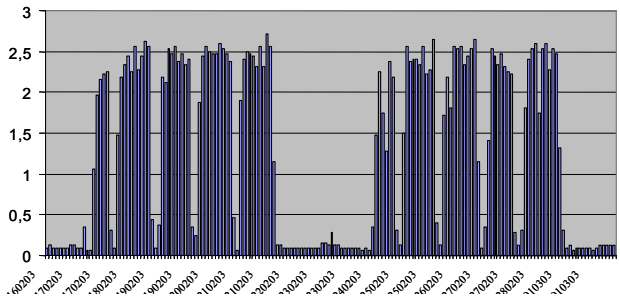
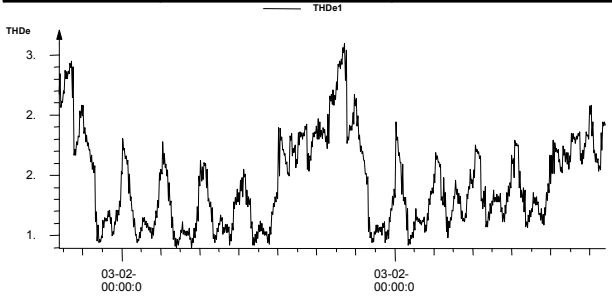


Figure 8. Chart of the long term flicker (Plt) of phase 1 with SVC; arc furnace working at 30 MW.

TABLE II. Summary of the single voltage per phase, minimum/maximum voltage and current harmonics values for the three phases.

PHASE-NEUTRAL VOLTAGE		
	MINIMUM	MAXIMUM
PHASE 1-N	122.250 V (ΔU= -3,74%)	132.410 V (ΔU= 4,26%)
PHASE 2-N	120.731 V (ΔU= -4,94%)	132.030 V (ΔU= 3,96%)
PHASE 3-N	122.107 V (ΔU= -3,85%)	132.552 V (ΔU= 4,37%)
VOLTAGE UNBALANCE	MINIMUM	MAXIMUM
	0,1 %	0,53 %
VOLTAGE HARMONICS		
THD	MINIMUM	MAXIMUM
PHASE 1	1,39 %	3,09 %
PHASE 2	1,22 %	3,17 %
PHASE 3	1,27 %	3,18 %
CURRENT HARMONICS		
THD	MINIMUM	MAXIMUM
PHASE 1	9,43 %	96,73 %
PHASE 2	7,06 %	73,83 %
PHASE 3	9,66 %	86,86 %



Maximum value/Minimum value of the voltage harmonic distortion Phase 1: 1,391644 % /3,0945771 %

Figure 9. Chart of Total Voltage Harmonic Distortion of Phase 1 with SVC; arc furnace working at about 30 MW.

V. CONCLUSIONS

Under normal conditions, but working at about 30 MW below the nominal power (83 MW) and with SVC we can conclude briefly:

Along the measurements campaigns for the working power of the arc furnace at about 30 MW the maximum value of the total voltage harmonic distortion at the measurement point of the factory was 3,18% (about 0,99% at the Carregado Substation) and the 95% of the harmonic factor values of the most significant harmonics are within the limits of standard EN50160. The maximum voltage harmonic factor value was 2,96%, corresponding to the 5th harmonic. The corresponding value at the Carregado substation will be about 0,92%. The maximum harmonic factor value for even harmonics, corresponding to the 2nd harmonic, was 0,369% (about 0,12% at the Carregado Substation) which is a very low value. In any case we must take into account that the arc furnace power is under the nominal power (about 37%).

The harmonic distortion of the current is dependent of Z(n) (inner impedance of the factory for each harmonic) and dependent of the SVC impedance, value of the load connected, amount and type of the materials, etc. This current harmonic distortion is very high and different for each phase. It is incredible but the maximum current harmonic factor value at the measurement point was 96,73%, which results in about 30,12% at the Carregado Substation. In reference [6] the authors conclude that with a SVC installed the Voltage Total Harmonic Distortion (THD) is practically the same (does not change) but the Current Total Harmonic Distortion nearly doubles. This is a consequence of the electronic devices that constitute the structure of the SVC.

The levels of flicker, long term flicker and short term flicker for 95% of the measurements values (Pst95%) in the Carregado Substation are just within the limits of the EN 50160 standard. The maximum value of Pst95% obtained at the factory measurement point was 3,313, 1,031 at the Carregado Substation. This value was produced the 19 of February, 2003, in phase 2, at a power of 30.690 kW.

Time-domain analysis of the arc furnaces with a three-phase circuit are quite costly concerning computation time, and those which are accomplished on a single phase circuit are not quite precise concerning harmonic content, mainly on the magnitude of zero sequence components.

ACKNOWLEDGEMENT

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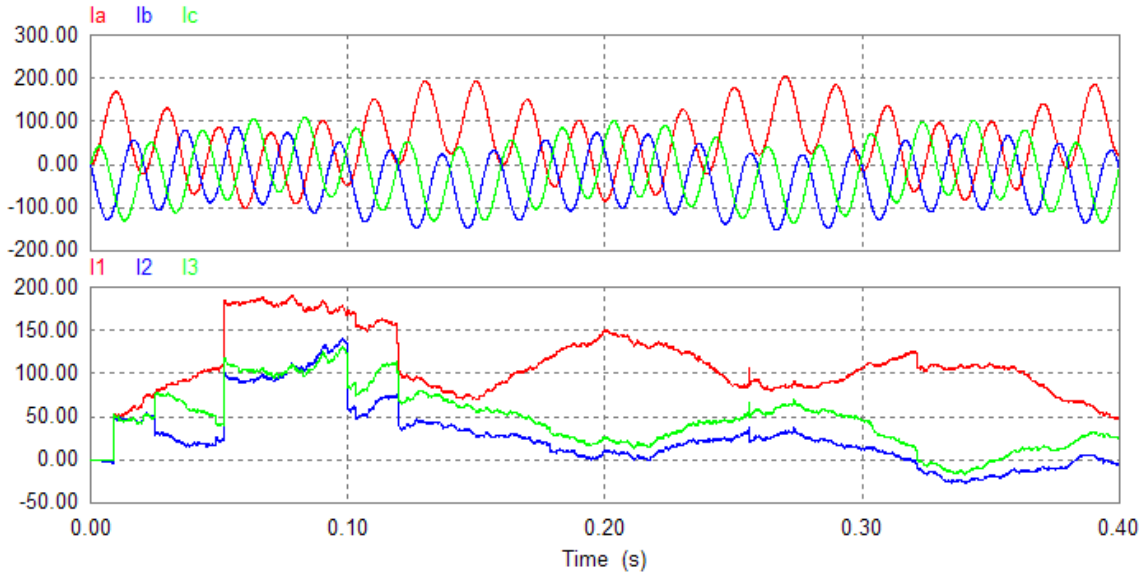

Figure 10. Input currents chart of the three phases and the chart of the currents that flow for each electrode of the AC arc furnace. All obtained using PSIM software with the circuit in Fig. 4.